AMENDMENTS TO THE CLAIMS

1. (Original) An embedded processor comprising:
a processing core having a processing core width;
a first memory component adjacent to a first side of the processing core;
a second memory component adjacent to the first memory component;
wherein the second memory component and the processing core are on opposite sides of the first memory component.

2. (Original) The embedded processor of claim 1, wherein the processing core width is equal to a first memory component width and a second memory component width.

3. (Original) The embedded processor of claim 1, wherein the first memory component if a cache.

4. (Original) The embedded processor of claim 3, wherein the second memory component is a scratch pad ram.

5. (Original) The embedded processor of claim 1, further comprising a third memory component adjacent to the second memory component, wherein the first memory component and the third memory component are opposite sides of the second memory component.

6. (Original) The embedded processor of claim 1, further comprising a third memory component adjacent to the processing core, wherein the third memory component and the first memory component are on opposite sides of the processing core.

7. (Original) The embedded processor of claim 6, wherein the first memory component is a data cache and the third memory component is a program cache.

8. (Original) The embedded processor of claim 6, wherein the first memory component is a cache and the third memory component is a scratch pad ram.

9. (Original) The embedded processor of claim 6, wherein the first memory component has a first memory size and the third memory component has a second memory size.

10. (Original) The embedded processor of claim 9, wherein the first memory size is not equal to the second memory size.

11. (Original) The embedded processor of claim 6, further comprising a fourth memory component adjacent to the third memory component, wherein the processing core and the fourth memory component are on opposite sides of the third memory component.

12. (Original) The embedded processor of claim 6, wherein the processing core width is equal to a first memory component width, a second memory component width, and a third memory component width.

13. (Original) The embedded processor of claim 1, wherein the first memory component has a first memory size and the second memory component has a second memory size.

14. (Original) The embedded processor of claim 13, wherein the first memory size is not equal to the second memory size.

15.-16. (Canceled)

17. (Currently Amended) A method of generating an embedded processor having a processing core, the method comprising:

selecting a plurality of memory components for the embedded processor;

configuring the memory components;

generating the memory components, wherein each memory component has a same width as the processing core;

placing a first memory component of the plurality of memory components adjacent to the processing core; and

~~The method of claim 16, further comprising~~ placing a second memory component of the plurality of memory components adjacent to the first memory component, wherein the processing core and the second memory components are on opposite sides of the first memory component.

18. (Original) The method of claim 17, further comprising placing a third memory component of the plurality of memory components adjacent to the second memory component, wherein the third memory component and the first memory component are on opposite sides of the second memory component.

19. (Original) The method of claim 17, wherein the first memory component is a cache and the second memory component is a scratch pad memory.

20. (Original) The method of claim 17, wherein the first memory component is a first scratch pad memory and the second memory component is a second scratch pad memory.

21. (Currently Amended) The method of claim 17 [[16]], further comprising placing a second memory component adjacent to the processing core, wherein the first memory component and the second memory components are on opposite sides of the processing core.

22. (Original) The method of claim 21, wherein the first memory component is a program cache and the second memory component is a data cache.

23. (Original) The method of claim 21, wherein the first memory component is a program cache and the second memory component is a scratch pad memory for data.

24. (Original) The method of claim 21, wherein the first memory component is a scratch pad memory for program instructions and the second memory component is a data cache.

25. (Original) The method of claim 21, further comprising placing a third memory component adjacent to the first memory component, wherein the third memory component and the processing core are on opposite sides of the first memory component.

26. (Original) The method of claim 25, further comprising placing a fourth memory component adjacent to the second memory component, wherein the fourth memory component and the processing core are on opposite sides of the second memory component.

27. (Currently Amended) The method of claim 17 [[15]], wherein the configuring the plurality of memory components comprises selecting a memory size for each memory component.

28. (Currently Amended) The method of claim 17 [[15]], wherein the configuring the plurality of memory components comprises selecting a number of ways for a first memory component, wherein the first memory component is a set associative cache.

29. (Currently Amended) The method of claim 17 [[15]], wherein the configuring a plurality of memory components comprises selecting a memory type for each memory component.

30.-31. (Canceled)

32. (Currently Amended) A system for generating an embedded processor having a processing core, the system comprising:

means for selecting a plurality of memory components for the embedded processor;

means for configuring the memory components;

means for generating the memory components, wherein each memory component has a same width as the processing core;

means for placing a first memory component of the plurality of memory components adjacent to the processing core; and

~~The system of claim 31, further comprising~~ means for placing a second memory component of the plurality of memory components adjacent to the first memory component, wherein the processing core and the second memory components are on opposite sides of the first memory component.

33. (Original) The system of claim 32, further comprising means for placing a third memory component of the plurality of memory components adjacent to the second memory component, wherein the third memory component and the first memory component are on opposite sides of the second memory component.

34. (Original) The system of claim 32, wherein the first memory component is a cache and the second memory component is a scratch pad memory.

35. (Original) The system of claim 32, wherein the first memory component is a first scratch pad memory and the second memory component is a second scratch pad memory.

36. (Currently Amended) A system for generating an embedded processor having a processing core, the system comprising:

means for selecting a plurality of memory components for the embedded processor;

means for configuring the memory components;

means for generating the memory components, wherein each memory component has a same width as the processing core; and

~~The system of claim 31, further comprising~~ means for placing a second memory component adjacent to the processing core, wherein the first memory component and the second memory components are on opposite sides of the processing core.

37. (Original) The system of claim 23, further comprising means for placing a third memory component adjacent to the first memory component, wherein the third memory component and the processing core are on opposite sides of the first memory component.

38. (Original) The system of claim 37, further comprising means for placing a fourth memory component adjacent to the second memory component, wherein the fourth memory component and the processing core are on opposite sides of the second memory component.

39. (Currently Amended) The system of claim 32 [[30]], wherein the means for configuring the plurality of memory components comprises means for selecting a memory size for each memory component.

40. (Currently Amended) The system of claim 32 [[30]], wherein the means for configuring the plurality of memory components comprises means for selecting a number of ways for a first memory component, wherein the first memory component is a set associative cache.

41. (Currently Amended) The system of claim 32 [[30]], wherein the means for configuring a plurality of memory components comprises means for selecting a memory type for each memory component.